For Sequential cells, the following characterizations have to be performed and filled.

1. **Input pin capacitances:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Input Pins** | **Rise Cap (pF)** | **Fall Cap (pF)** | **Average Cap (pF)** |
| D | 0.00323171388 | 0.00324560581 | 0.00323865984 |
| CLK | 0.0116678248 | 0.01157309179 | 0.01162045829 |

1. **Set-up Time Table:**

**(i) Rise Constraint** **(in ns)** [Input slew vs CLK slew].

|  |  |  |
| --- | --- | --- |
| **Input\CLK** | **10 ps** | **1000 ps** |
| **10 ps** | 0.10 | 0.7 |
| **1000 ps** | 0.73 | 0.15 |

**(ii) Fall Constraint** **(in ns)** [Input slew vs CLK slew].

|  |  |  |
| --- | --- | --- |
| **Input\CLK** | **10 ps** | **1000 ps** |
| **10 ps** | 0.12 | 0.71 |
| **1000 ps** | 0.75 | 0.16 |

1. **Hold Time Table:**

**(i) Rise Constraint** **(in ns)** [Input slew vs CLK slew].

|  |  |  |
| --- | --- | --- |
| **Input\CLK** | **10 ps** | **1000 ps** |
| **10 ps** | 0 | 0 |
| **1000 ps** | 0 | 0 |

**(ii) Fall Constraint** **(in ns)** [Input slew vs CLK slew].

|  |  |  |
| --- | --- | --- |
| **Input\CLK** | **10 ps** | **1000 ps** |
| **10 ps** | 0 | 0 |
| **1000 ps** | 0 | 0 |

1. **Transition Time Table (for Q output, CLK will have minimum slew of 10 ps):** (please strictly consider 20% and 80% of VDD for transition time)

**(i) Output Rise Transitions** **(in ns)** [Input slew vs output capacitance].

**Related pin D**: (i.e., other input pins are held constant)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **10 ps** | **100 ps** | **1000 ps** |
| **0.5 fF** | 2.614960e-11 | 2.614960e-11 | 2.614960e-11 |
| **10 fF** | 7.199715e-11 | 7.199715e-11 | 7.199715e-11 |
| **100 fF** | 5.513904e-10 | 5.513904e-10 | 5.513904e-10 |

**(ii) Output Fall Transitions** **(in ns)** [Input slew vs output capacitance].

**Related pin D**: (i.e., other input pins are held constant)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **10 ps** | **100 ps** | **1000 ps** |
| **0.5 fF** | 2.233923e-11 | 2.233923e-11 | 2.233923e-11 |
| **10 fF** | 7.980830e-11 | 7.980830e-11 | 7.980830e-11 |
| **100 fF** | 6.428031e-10 | 6.428031e-10 | 6.428031e-10 |

1. **CLK-to-Q Delay Time Table**: (delay between clock transition and data transition. Use 50% of CLK to 50% of output to simulate propagation delay).

**(i) Cell Rise Delay (in ns)** [Input slew vs output capacitance].

**Related pin D**: (i.e., other input pins are held constant)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **10 ps** | **100 ps** | **1000 ps** |
| **0.5 fF** | 2.475187e-10 | 2.475187e-10 | 2.475187e-10 |
| **10 fF** | 2.960196e-10 | 2.960196e-10 | 2.960196e-10 |
| **100 fF** | 6.305038e-10 | 6.305038e-10 | 6.305038e-10 |

**(ii) Cell Fall Delay (in ns)** [Input slew vs output capacitance].

**Related pin D**: (i.e., other input pins are held constant)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **10 ps** | **100 ps** | **1000 ps** |
| **0.5 fF** | 1.643064e-10 | 1.643064e-10 | 1.643064e-10 |
| **10 fF** | 2.220352e-10 | 2.220352e-10 | 2.220352e-10 |
| **100 fF** | 6.599945e-10 | 6.599945e-10 | 6.599945e-10 |

1. **Static Power (all possible input combinations of CLK and D).**

|  |  |
| --- | --- |
| **Condition (CLK, D)** | **Power (nW)** |
| 00 | 6531.675 |
| 01 | 0.611568 |
| 10 | 5345.84 |
| 11 | 5334.35 |

1. **Dynamic Power Table: (CLK will have minimum slew of 10 ps)**

**(i) Rise Power (in nW)** [Input slew vs output capacitance].

**Related pin D**: (i.e., other input pins are held constant)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **10 ps** | **100 ps** | **1000 ps** |
| **0.5 fF** | 0.060912 | 0.0765 | 0.0378 |
| **10 fF** | 0.02484 | 0.019872 | 0.01638 |
| **100 fF** | 0.00864 | 0.0702 | 0.00306 |

**(ii) Fall Power (in nW)** [Input slew vs output capacitance].

**Related pin D**: (i.e., other input pins are held constant)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **10 ps** | **100 ps** | **1000 ps** |
| **0.5 fF** | 0.216 | 0.00864 | 0.0038556 |
| **10 fF** | 0.05346 | 0.054 | 0.0309771 |
| **100 fF** | 0.00297 | 0.00081 | 0.004176 |